

Applicant : Narain D. Arora, et al.  
Appl. No. : 10/806,680  
Examiner : Sun J. Lin  
Docket No. : 700693.4026

**Amendment to the Drawings**

Attached herewith are corrected drawings for Figures 1-4 to replace the original drawings for Figures 1-4. Specifically, the following corrections were made to the drawings:

In Fig. 2B, item "Ground 205" has been deleted.

In Fig. 4, the dashed line has been deleted.

In Fig. 1 – Fig. 4, the labels have been typed.

Attachment: Replacement Sheet

Applicant : Narain D. Arora, et al.  
Appl. No. : 10/806,680  
Examiner : Sun J. Lin  
Docket No. : 700693.4026

### **Remarks**

Claims 1, 6, 11, 18 and 22 have been amended, claim 2 has been cancelled, and new claims 31 and 32 have been added. Claims 1 and 3-32 are pending in the application. Reconsideration of the application as amended herein is respectfully requested.

### **Drawing Objections**

The drawings were objected to because of the following informalities:

Fig. 2B delete item "Ground 205"

Fig. 4, meaning of dashed line connecting Vss G is not clear.

Due to poor hand writing, many labels shown in Fig. 1 – Fig. 4 are not readable.

Applicants have made the following correction to the drawings (attached herewith as replacement sheets):

In Fig. 2B, item "Ground 205" has been deleted.

In Fig. 4, the dashed line has been deleted.

In Fig. 1 – Fig. 4, the labels have been typed.

Therefore, Applicants submit that the objections to the drawings have been overcome.

### **Claim Objections**

Claim 1 was objected to because of the following informalities:

Claim 1, line 5, after "first" insert – conductor –.

Applicants respectfully traverse this objection because "first" properly refers to the "first set of coupling capacitances" and not to a first conductor.

### **Claim Rejections – 35 U.S.C. §102**

Claims 11-19 and 21-30 were rejected under 35 U.S.C. § 102(a) as being unpatentable over IEEE Paper entitled "Non-Destructive Inverse Modeling of Copper Interconnect Structure for 90nm Technology Node" authored by Kunikiyo et al. (hereinafter "Kunikiyo"). Applicants respectfully traverse.

Applicant : Narain D. Arora, et al.  
Appl. No. : 10/806,680  
Examiner : Sun J. Lin  
Docket No. : 700693.4026

Independent claim 11 has been amended to recite "wherein the first capacitance and second capacitance are determined **separately**" (emphasis added). Support for this amendment can be found, for example, in paragraph [0030] on page 11 of the specification, in which capacitances  $C_t$  and  $C_b$  are determined **separately**, i.e., separate capacitance values are determined for  $C_t$  and  $C_b$ . In this example embodiment, seven capacitances  $C_1$ - $C_7$  are measured and the resultant capacitance measurements are plugged into two separate equations 1 and 2 to determine  $C_t$  and  $C_b$  **separately**.

Claim 11, as amended, is patentable over Kunikiyo because Kunikiyo fails to disclose, teach or suggest determining the first capacitance and the second capacitance **separately**. Rather, the measurement procedure of Kunikiyo can only be used to determine the **total** inter-level capacitance  $C_v = C_{up} + C_{low}$ , which is the sum of  $C_{up}$  and  $C_{low}$ . Kunikiyo does not determine the capacitance of  $C_{up}$  and  $C_{low}$  **separately**, i.e., does not determine separate capacitance values for  $C_{up}$  and  $C_{low}$ . The measurement procedure of Kunikiyo only makes two capacitance measurements of a test structure, one with selection signal  $SEL = V_{ss}$  and one with  $SEL = V_{dd}$  (see Kunikiyo, Section II). The two capacitance measurements are:

$$C_{total}(SEL = V_{ss}) = (2n \times C_c + n \times C_v) \times L + \alpha; \text{ and}$$

$$C_{total}(SEL = V_{dd}) = (2 \times C_c + 2n \times C_v) \times L + \beta.$$

In order to determine  $C_v$  and  $C_c$  (coupling capacitance between comb structures), Kunikiyo makes these two capacitance measurements for each of two different test structures having different overlap lengths,  $L$ , and solves four simultaneous equations based on these measurements (see page 32, third paragraph). Kunikiyo does **not** determine  $C_{up}$  and  $C_{low}$  **separately**, only the sum  $C_v = C_{up} + C_{low}$ . In fact, it is impossible to determine  $C_{up}$  and  $C_{low}$  separately from the capacitance measurements taken by Kunikiyo. Further, the measurement circuit of Kunikiyo is **not** electrical connected to the top and bottom plates of the test structure making it impossible to determine  $C_{up}$  and  $C_{low}$  **separately** using the measurement circuit of Kunikiyo (see Figures 1 and 2). The top and bottom plates are either grounded or left floating.

The invention of claim 11 has many advantages over Kunikiyo, including the fact that the claimed subject matter allows extraction of process parameters for interconnect lines having different top and bottom surface widths, e.g., trapezoidal cross sections. This is because an interconnect line having different top and bottom surface widths forms different top and bottom

Applicant : Narain D. Arora, et al.  
Appl. No. : 10/806,680  
Examiner : Sun J. Lin  
Docket No. : 700693.4026

capacitance structures with the top and bottom plates. By determining the top and bottom capacitances **separately**, the invention of claim 11 allows the extraction of process parameters for the interconnect line having different top and bottom surface widths using a single test structure. Kunikiyo does not possess this advantage because Kunikiyo only determines the sum  $C_v = C_{up} + C_{low}$ , with no means of separating  $C_{up}$  and  $C_{low}$ . It is impossible to determine  $C_{up}$  and  $C_{low}$  separately using the methods of Kunikiyo, and therefore impossible to extract process parameters when the top and bottom capacitances are different due to different line widths at the top and bottom surfaces. In fact, Kunikiyo assumes that the interconnect lines have rectangular cross sections, i.e.,  $C_{up} = C_{low}$ .

Therefore, Applicants submit that independent Claim 11 is patentable over Kunikiyo. Chou (U.S. Pat No. 6,312,963 B1) fails to teach or suggest the deficiencies of Kuyikiyo. Therefore, Applicants also submit that independent Claim 11 is not rendered obvious by the combined teachings of Kunikiyo and Chou.

Dependent Claims 12-19 and 21 are patentable by virtue of their dependence on Claim 11.

Claim 22 has been amended to recite "a first multiplexer circuit connected to the first conductive plate; a second multiplexer circuit connected to the second conductive plate; and a CBCM circuit connected to the first multiplexer circuit and the second multiplexer circuit." Claim 22 is patentable because neither Kunikiyo nor Chou, either alone or in combination, teaches or suggests connecting the top and bottom plates to multiplexer circuits, much less multiplexer circuits connected to a CBCM. Therefore, Applicants submit that Claim 22 is patentable.

Dependent Claims 23-30 are patentable by virtue of their dependence on Claim 22.

### **Claim Rejections – 35 U.S.C. §103**

Claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kunikiyo in view of Chou et al. (U.S. Pat No. 6,312,963 B1). Applicants respectfully traverse.

Claim 1 has been amended to recite "determining a first capacitance between a first plate and a first conductor or a second conductor; and determining a second capacitance between a second plate and the first or the second conductor, wherein the first capacitance and the second

Applicant : Narain D. Arora, et al.  
Appl. No. : 10/806,680  
Examiner : Sun J. Lin  
Docket No. : 700693.4026

capacitance are determined separately" (emphasis added). The importance of this and the fact that Kunikiyo fails to disclose this feature is discussed above. Applicants respectfully submit that Chou fails to teach or suggest anything remotely similar to independent capacitance determinations. Therefore, Applicants submit that Claim 1 is patentable for the reasons given above for Claim 11.

Claims 2-9 are patentable by virtue of their dependence on Claim 1.

### **New Claim**

New Claim 31 depends from claim 11 and is therefore patentable for at least the reasons given for claim 11. Claim 31 is additionally patentable because Kunikiyo does not teach or suggest "determining the first capacitance and the second capacitance separately based on capacitance measurements of a **single** test structure." As discussed above, Kunikiyo does not even teach or suggest determining  $C_{up}$  and  $C_{low}$  **separately**, much less based on capacitance measurements of a **single** test structure. In fact, the measurement procedure of Kunikiyo requires capacitance measurements of **two** different test structures having different overlap lengths to determine  $C_c$  and  $C_v$  (see Kunikiyo, page 32, third paragraph).

### **Allowable Subject Matter**

Applicants appreciate the Examiner's indication that Claim 20 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Applicants have rewritten claim 20 as claim 32 so that it includes all the limitations its base claim 11 had prior to amendment.

### **Conclusion**

Applicants respectfully submit that this application is in condition for allowance, which is respectfully requested. Should the Examiner have any questions or comments on the application, the Examiner should feel free to contact the undersigned via telephone.

The Commissioner is authorized to charge any fee which may be required in connection with this Amendment to deposit account No. 15-0665.

Applicant : Narain D. Arora, et al.  
Appl. No. : 10/806,680  
Examiner : Sun J. Lin  
Docket No. : 700693.4026

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: 2/27/06

By: Eugene Worley  
Eugene Worley  
Reg. No. 47, 186

Orrick, Herrington & Sutcliffe LLP  
4 Park Plaza, Suite 1600  
Irvine, CA 92614-2558  
Tel. 650-614-7622  
Fax: 949-567-6710